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Tunnel Field Effect Transistor (TFET) I-V Characteristics and C-V Characteristics Approximation

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Abstract: Tunnel Field Effect Transistor (TFET) has been extensively investigated in recent decades. TFETs set an alternative to conventional transistors. TFETs are based on diverse operating principles that include tunneling. Steep Sub threshold swing transistors based on tunneling are examined to extend the performance of a transistor. Tunnel FET is having a lesser on current, off current and Sub threshold slope than conventional MOSFETs which is found to be a latent candidate for ultra-low power device applications by the reduced sub threshold swing. This leads to the reduction of supply voltage; thereby it increases the speed of the devices.

Index Terms: Subthreshold Swing, Quantum tunneling, On Current, Off Current.

I. INTRODUCTION

Advancements in VLSI technology have led to the doubling of transistors on a silicon chip after every 24 months according to Moore's law. The main aim of electronics is "miniaturization". The "Moore's Law" is a description of the periodic increase in the level of miniaturization. Very large scale integrated circuits (VLSI) are the process of incorporating ICs by combining thousands of transistors into a single chip. The previous integrated circuits design method involves SSI means Small Scale Integrated Circuits in which circuits held only a few devices, perhaps as ten diodes, transistors, resistors and capacitors. MSI means medium scale integration. This technique led to devices with hundreds of logic gates. LSI means large scale integration i.e. systems with at least a thousand logic gates. Integrated circuits are constructed using CMOS technology (Complementary Metal Oxide Semiconductor). It finds application in Microprocessors, Microcontrollers, Static RAM and digital circuits As the CMOS technology is enriched, device structure is scaled to Nano meter range in order to obtain high speed, less area, low power consumption.
The increasing want for an efficient energy electronics calls for an alternative device concepts TFET is an electron device of next generation owing to its smaller sub threshold swing. TFET having a potential to exceed the 60mV/decade sub-threshold swing, increases Speed due to tunneling effects. It also have an ability to work on sub threshold voltage and its fabrication is much closer to the fabrication of MOSFET.

II. BACKGROUND

The main challenge of CMOS logic is to improve the performance of the device and reduced power consumption. With a large density of small transistor geometries and fast clock speeds the need to address issues with both dynamic and static power has arisen. Dynamic power is relation to CfV_{DD}^2, whereas C is the load capacitance and f is the frequency, V_{DD} is the supply voltage. Reducing the supply voltage is the best approach to reducing dynamic power due to the squared dependence. The processor clock speeds have remained mostly constant over the past few generations so as to not consume more power. Acting against the power savings is the increased gate capacitance that is a result of thinning the gate oxide to smaller Equivalent oxide thicknesses (EOT).
Addressing the static power requires an examination of gate leakage currents and switching characteristics. Gate leakage is being addressed using high-k gate dielectrics which allow for thicker films which reduce the tunneling through the gate oxide while maintaining the same electrostatic control. To minimize losses during switching a steep switching slope, S, and small voltage range is preferable [4]. The reduction of S and V_{dd} are both addressed by using the Tunnel field-effect transistor (TFET) which uses quantum mechanical band-to-band tunneling (BTBT) as the current transport mechanism.
To further understand the impulse for the TFET it is useful to provide a deeper investigation into the scaling limitations of MOSFETs, particularly pertaining to the switching characteristic as Vdd is reduced. Since a large on current is needed to drive logic operations Vdd must be sufficiently larger than the threshold voltage, V_t, to provide the necessary

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current modulation to drive the next stage while still maintaining a distinct off-state. This requires that the difference between the on (I_{ON}) and off (I_{OFF}) current states span several orders of magnitude. Therefore V_t must also be reduced with scaling to provide a sufficient gate overdrive and maintain performance. However, with Vdd reduced, the voltage margin that the transistor has to switch between the off and on-state is also reduced.

III. TUNNEL FIELD EFFECT TRANSISTOR

The structure of TFET is common P-I-N structure; source and the drain terminals are heavily doped while the semiconductor layer is lightly doped whereas the gate terminal controls the electrostatic potential the concentration of charge get increases in the junction between the semiconductor wafer and P-type region. TFET involves the lower ON current due to the reverse biased P-I-N structure. The switching mechanism of TFET involves tunneling. As a result, under sufficient gate bias voltage, a strong band bending is formed such that the electrons can tunnel from the valence band of p-region to the conduction band of intrinsic region. This process is termed as band-to-band tunneling (BTBT) and the tunneling current is the on-current of TFET device.

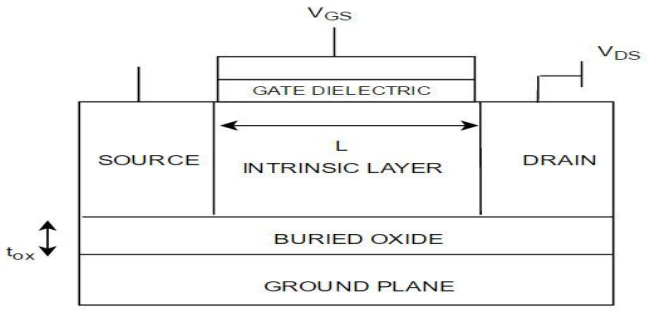

Figure 1. Schematic cross section of n-type TFET

When there is no applied Vgs, a wide barrier exists at the source-channel junction, that is ideally the length of the channel, and negligible tunneling occurs .When a positive bias is applied, the bands in the intrinsic region are pushed down creating a channel that begins to appear n-type. As Vgs is further increased the energy barrier is reduced until the tunneling probability increases conversely to the nTFET, the source in the pTFET is the n-region which allows for injection of holes into the channel. In n-TFET, electron tunnels from the valence band in source to the conduction band in drain while in p-TFET, the holes tunnel from the conduction band in source to the valence band in drain. Band to band tunneling depends on the barrier height and width.

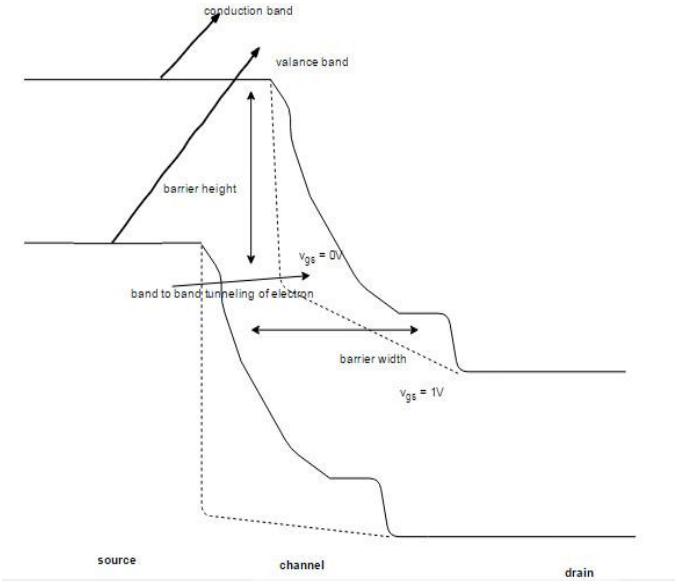

Figure 2. Tunneling diagram of TFET

When the gate source voltage is zero, width of the channel is higher, hence no possibility for band to band tunneling to occur.

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A. BAND TO BAND TUNNELING OF TFET

Aimed at band to band tunneling, the essential condition is the total voltage drop across. The Band to Band Tunneling phenomenon provides an expression for the tunneling Transmission of carriers and can be achieve by Wentzel Kramers Brillouin (WKB) Approximation and considering the tunnel barrier as a triangular shaped potential Barrier According to WKB approximation, the Band to Band Tunneling transmission is given by the following expression.

$$Tt \approx \exp\left[-2\int |k(x)| dx - x_2 x_1\right] \quad (1)$$

Where k(x) is the quantum wave vector of the electron inside the triangular barrier and given by,

$$K(x) = (2m^*/h^2\ (PE-E))^{1/2} \quad (2)$$

Where m* is the electron effective mass and is Planck's constant divided by 22π. The term E is zero at width of the triangle. The rate of reduction in PE can be represented as

$$(Eg/2\text{-}qFx) \quad (3)$$

Where Eg is the band gap of the semiconductor material at the tunnel junction, and F is the electric field measured in V/m, the new term (F) has the unit of eV/m, we must also cancel out an electron charge,

$$K(x) = (2m^*/h^2\ (Eg/2\text{-}qFx))^{1/2} \quad (4)$$

Now this expression can be used with equation (1) to obtain the expression below:

$$Tt \approx \exp\left[-2\int \sqrt{2m*/h(Eg^2 - qFx)dx - x_2 x_1}\right] \quad (5)$$

Looking back at the triangular barrier, we know that at

$$X=Eg$$

and that at X=0

$$Tt \approx \exp\left(-4/3\ ((2m^*)\ 0.5/qFh)\ Eg^{3/2}\right) \quad (6)$$

The TFET acts as a band pass filter that cuts of the low-energy and high-energy tails of the Fermi distribution of the P-type source and channel region respectively.

Rearranging the equation, the following is obtained,

$$Tt \approx \exp\left(-4\lambda/3\ \sqrt{2m*/h(\Delta\emptyset + Eg)(Eg)^{3/2}}\right) \quad (7)$$

B. MODELING OF TFET

Tunnel FET can be modeled based on their surface and electric potential. The surface potential in the gate oxide region. The electric-field potential is along the channel length. Based on the kanes approximation model the modeling of TFET can be done.

1. Surface potential:

The 2D Poisson equation can be represented as,

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = \frac{qNA}{\varepsilon Ge} \quad (8)$$

Where q is the electric charge and εGe is the Ge permittivity.

The boundary conditions of poisson equations are,

(a) Electric flux at gate oxide interface,

$$\frac{d\phi(x,y)}{dy} = \frac{\varepsilon_{ox}}{\varepsilon_{Ge}} \frac{\phi_s(x) - \psi_g}{t_{ox}},\ y=0 \quad (9)$$

(b) Electric flux at gate oxide and channel interface,

$$\frac{d\phi(x,y)}{dy} = 0,\ y = t_{Ge} \quad (10)$$

The order of polynomial is two,

$$\phi(x,y) = c_0(x) + c_1(x)y + c_2(x)y^2 \quad (11)$$

Whereas co (x), c_1 (x) and c_2 (x) are arbitrary constants.

$$c_0(x) = \phi_s(x) \quad (12)$$

$$c_1(x) = \frac{\phi_s(x) - \psi_g}{t_{ox}} \frac{\varepsilon_{ox}}{\varepsilon_{Ge}} \quad (13)$$

$$c_2(x) = \frac{1}{2t_s} \frac{\varepsilon_{ox}}{\varepsilon_{Ge}} \frac{\psi_g - \phi_s(x)}{t_{Ge}} \quad (14)$$

Substituting the values of co (x), c_1 (x) and c_2 (x) in polynomial equation and obtained potential distribution as,

$$\varphi_s(x) = Ae^{\lambda x} + Be^{-\lambda x} + \psi_g \quad (15)$$

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Where,

$$\lambda = \sqrt{\frac{\varepsilon_{ox}}{\varepsilon_{Ge}\ t_{ox}\ t_{Ge}}}$$

the coefficients A and B can take the values as,

$$A = \frac{-1}{2\ sin\ h(\lambda L)} \times [V_{bi}\, e^{-\lambda L} - (V_{bi} + V_{DS}) + \psi_g(1 - e^{-\lambda L}) + V_{DS}] \quad (16)$$

$$B = \frac{1}{2 \sin h(\lambda L)} \times [\, V_{bi}\, e^{\lambda L} - (\, V_{bi} + V_{DS}) + \psi_g\, (1 - e^{\lambda L}) - V_{DS}\,] \quad (17)$$

2. Electric field

The electric field along the channel can be represented as E_x and E_y,

$$E_x = -\frac{d\phi_s(x)}{dx} = -(A\lambda e^{\lambda x} - B\lambda e^{-\lambda x}) \quad (18)$$

$$E_y = -\frac{d\phi_s(x)}{dx} = -[\, C_1(x) + 2yC_2(x)] \quad (19)$$

3. Drain current

The drain current can be obtained by integrating generation rate (G) using kanes model,

$$I_d = q \int G dx dy \quad (20)$$

$$G(E) = A \frac{|E|^2}{\sqrt{E_G}} \exp(-B \frac{E_g{}^{3/2}}{|E|}) \quad (21)$$

Where |E| is the magnitude as $\sqrt{E_x^2 + E_y^2}$ and E_g is the energy gap.

IV. SUBTHRESHOLD SWING OF TUNNEL FET

In order to describe the expression for the sub-threshold swing of a band-to-band tunneling device, consider the Band to Band Tunneling current is given below for reverse-biased p-n junction,

$$I = aV_{eff}\, E e^{-b/E} \quad (22)$$

Where,

$$a = Aq^3\, (\sqrt{2m*/Eg})/\pi^2 h^2 \quad (23)$$

Where A is the device cross sectional area and

$$b = 4\sqrt{m*}\ Eg^{3/2}/3qh \quad (24)$$

V_{eff} is the bias at the tunnel junction and E is the electric field at the tunnel junction and the sub-threshold swing is calculated as,

$$SS = dVgs/d\,(logIds) \quad (25)$$

$$SS = \ln(10)\, [(1Veff/dveff/dvgs) + (E+b)/E*E\ dE/dVgs]^{-1} \quad (26)$$

The second term describes that the derivative of the junction electric field on the gate-source voltage should be maximized.

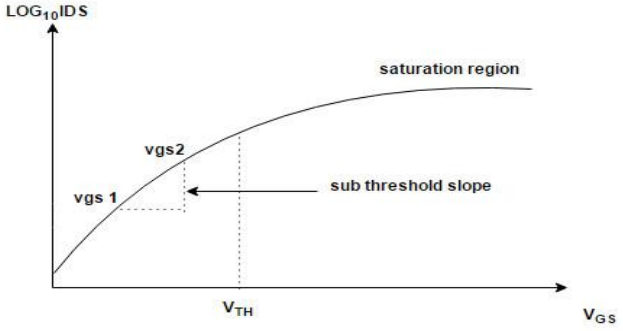

Figure 3. Subthreshold Swing plot

Accordingly, the sub-threshold swing in a TFET increases with gate-source voltage and much steeper at lower gate voltages [4].

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As the transistor gate length is reduced, improved performance requires the supply voltage, VDD, and simultaneously the threshold voltage, V_t, to be lowered to keep the overdrive factor ($V_{DD} - V_T$) high.
Another way of reducing the voltage supply without performance loss is to increase the turn-on steepness, which means decreasing the average sub threshold swing, S_{avg} defined as,

$$S_{avg} = VT\text{-}VG_{OFF}/\log (I_t/I_{OFF}) \approx V_{DD}/\log (I_{ON}/I_{OFF}) \quad (27)$$

V. RESULT AND SIMULATION

Various parameters of TFET include channel length, width, doping concentration, oxide material, thickness, bias.

Table 1. Various parameters of TFET and their specifications

PARAMETERS	VALUES
Channel length	50nm
Device doping	$1.0x10^{17}cm^{-3}$
Device layer thickness	10nm
Gate oxide material	$SiO_2$and HfO_2
Gate oxide thickness	1nm to 6nm
Device width	10nm to 50nm
Gate bias	1v
Drain bias	1v

By the varied parameters of TFET, the current voltage characteristics are obtained in MATLAB. Consider the TFET Id-Vg characteristic for work function = 4.2 eV shown in figure to explain its tunneling current behaviour.

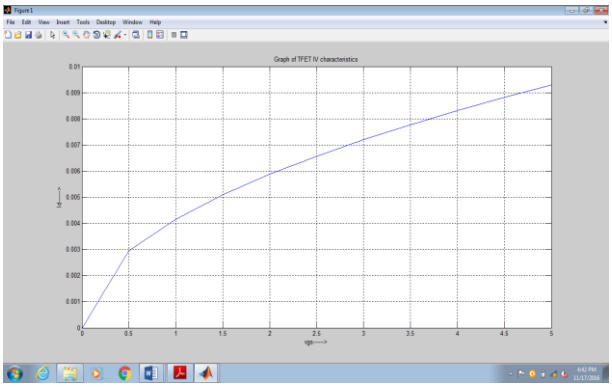

Figure 4. Plot against Vgs and Id

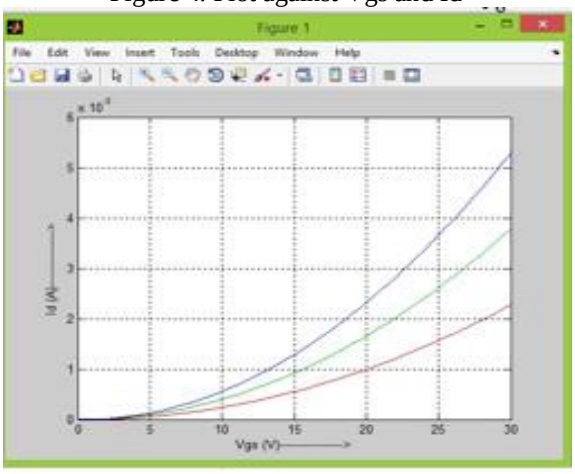

Figure 5. Plot for various gate-source voltage

The saturation current or ON current of TFET,

$$Vgs > Vt,$$
$$I_D = 1/2\ \mu_n\ Cox\ W/L\ (VGS\text{-}Vth)\ 2\ (1+ \lambda\ Vds) \quad (28)$$

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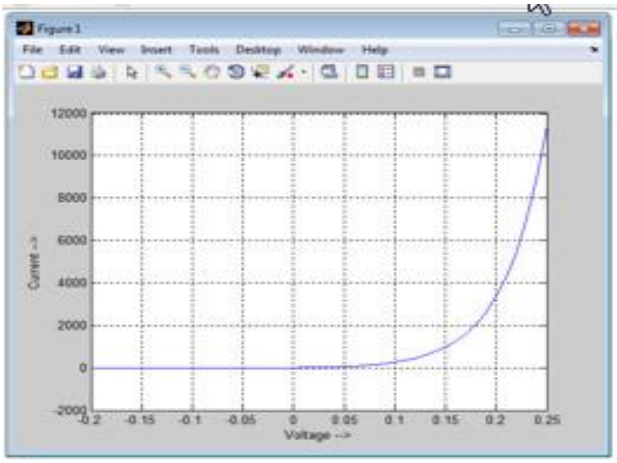

Figure 6. Parabolic MATLAB simulation for IV characteristics

Where λ is the channel length modulation if λ =0,

$$I_D=1/2\ \mu_n\ Cox\ W/L\ (VGS-Vth)^2 \qquad (29)$$

The above Figures Shows the obtained Current-Voltage characteristics of TFET for the above saturation current equation in matlab using parameters of TFET.

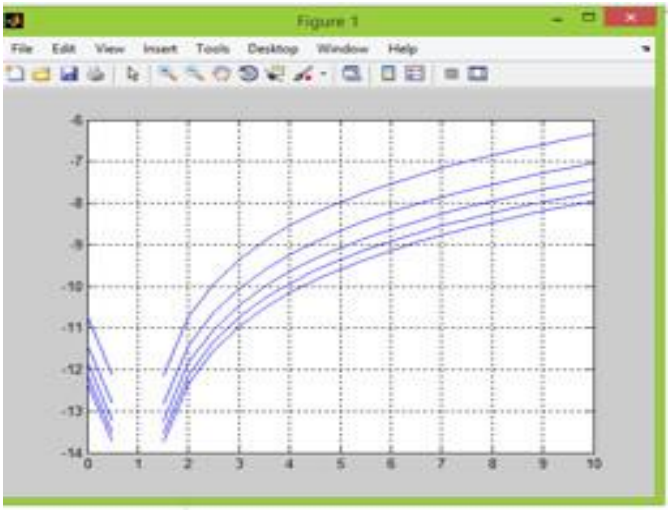

Figure 7. TFET in sub threshold voltage region

It is clearly observed that Vt is shifting towards right as we increase the work function of the metal of the gate. For the higher gate metal work function, the conduction band of the channel shifted upwards. In order to push it downwards towards the valance band of source, more gate voltage is needed to start the tunneling which increases the Vt of the device. It is clearly shown from the figure that for lower gate voltages TFET showing its steep threshold behavior. This reduced the sub-threshold leakage for electronic devices in standby mode.

The TFET with the 100nm channel length and the 3nm gate oxide thickness is simulated. The drain is n+ doped with the doping level of 1×10^{19} cm^{-3} and the p type source doping level is $1\times10^{20}cm^{-3}$.In our MOSFET simulation, the sub threshold swing smaller than 60mv/dec is never observed in any region. This simulation proves that the sub threshold swing in TFET is not limited by

$$\ln (10) \cdot kT/q$$

the channel length is 100nm and tox =3nm.

Gate capacitances are extracted by computing the change in gate charge with respect to a small change in terminal voltage at each bias,

$$Cgd = \partial Qg/\partial Vd|Vs,Vg\ , \qquad (30)$$

$$Cgs = \partial Qg/\partial Vs|Vd,Vg \quad \text{and}$$

$$Cgg = \partial Qg/\partial Vg|Vs,Vd \qquad (31)$$

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In Figure 8, the simulated C-V characteristics of N-TFET are shown. The one and only motivation of these C-V simulations to analyze the high miller capacitance effect in TFET due to large values of Cgd.

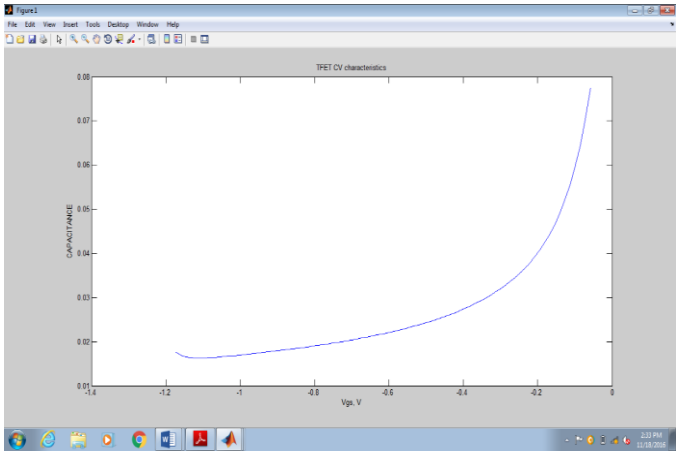

Figure 8. C-V characteristics of TFET

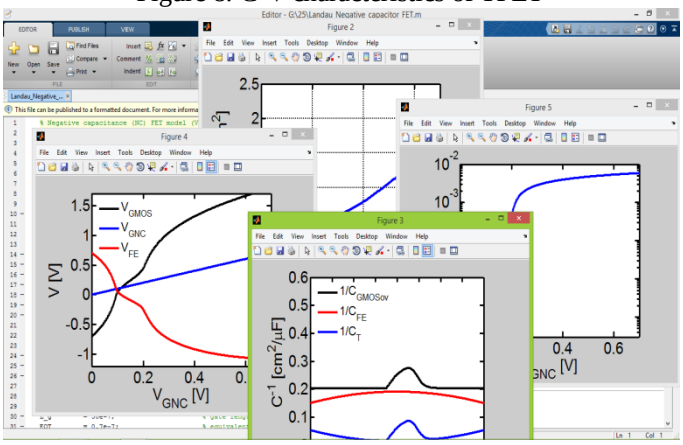

Figure 9. The various curves against the characteristics of capacitance

VI. CONCLUSION AND FUTURE WORK

The result of this paper against TFET involves lower sub threshold swing. TFETs also provide additional performance benefits in terms of both energy and delay for logic designs. Steep Sub threshold swing transistors based on tunneling are obtained to dominate the performance of a MOS transistor [8]. The obtained I-V and C-V characteristics are then stored in a 2-D look up table for use in simulations. Since analytical models for TFETs are not readily available, therefore the best way for circuit simulations is to build a Look up table based model using Verilog-A. Verilog-A module is then used as instances for circuit simulations in Cadence Specter [3].

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